

CLAIMS

What is claimed is:

1 1. A method of processing for a semiconductor device,
2 the method comprising:
3 providing a wafer including a substrate;
4 forming a plurality of sidewalls around a plurality of
5 cylindrical pedestals above a surface of the substrate;
6 removing the plurality of cylindrical pedestals; and
7 vertically etching horizontal surfaces of a first
8 material located around the plurality of sidewalls.

1 2. The method of claim 1, wherein,
2 the plurality of sidewalls provide an etch stop.

1 3. The method of claim 2, wherein,
2 the plurality of sidewalls protect the first material
3 under the plurality of sidewalls from being etched during the
4 vertical etching of the first material.

1 4. The method of claim 1, further comprising:
2 removing the plurality of sidewalls.

1 5. The method of claim 1, further comprising:
2 diffusing a dopant into the first material located
3 around the plurality of sidewalls.

1 6. The method of claim 1, further comprising:
2 diffusing a dopant into a second material around the
3 plurality of sidewalls.

1 7. The method of claim 1, further comprising:
2 diffusing a dopant into the first material and a second
3 material around the plurality of sidewalls.

1 8. The method of claim 1, further comprising:
2 diffusing a dopant into the first material or a second
3 material around the plurality of sidewalls.

1 9. The method of claim 8, wherein,
2 the plurality of sidewalls provide an etch stop and a
3 diffusion barrier.

1 10. The method of claim 9, wherein,
2 the plurality of sidewalls protect the first material
3 under the plurality of sidewalls from receiving a dopant
4 during the diffusing of the dopant into the first material or
5 the second material.

1 11. The method of claim 9, wherein,
2 the plurality of sidewalls protect the second material
3 under the plurality of sidewalls from receiving a dopant

4 during the diffusing of the dopant into the first material
5 and the second material.

1 12. The method of claim 9, wherein,
2 the plurality of sidewalls protect the first material
3 and the second material under the plurality of sidewalls from
4 receiving a dopant during the diffusing of the dopant into
5 the first material or the second material.

1 13. A method of processing for a semiconductor device,
2 the method comprising:
3 providing a wafer including a substrate;
4 forming a plurality of sidewalls around a plurality of
5 cylindrical pedestals above a surface of the substrate;
6 removing the plurality of cylindrical pedestals; and
7 diffusing a dopant into a first material located around
8 the plurality of sidewalls.

1 14. The method of claim 13, wherein,
2 the plurality of sidewalls provide a diffusion barrier.

1 15. The method of claim 14, wherein,
2 the plurality of sidewalls protect the first material
3 under the plurality of sidewalls from receiving a dopant
4 during the diffusing of the dopant into the first material.

1 16. The method of claim 13, further comprising:

2 removing the plurality of sidewalls.

1 17. The method of claim 13, further comprising:
2 vertically etching horizontal surfaces of the first
3 material located around the plurality of sidewalls.

1 18. The method of claim 13, further comprising:
2 vertically etching horizontal surfaces of a second
3 material located around the plurality of sidewalls.

1 19. The method of claim 13, further comprising:
2 vertically etching horizontal surfaces of the first
3 material and a second material located around the plurality
4 of sidewalls.

1 20. The method of claim 13, further comprising:
2 vertically etching horizontal surfaces of the substrate
3 located around the plurality of sidewalls.

1 21. The method of claim 13, further comprising:
2 vertically etching horizontal surfaces of the first
3 material or a second material located around the plurality of
4 sidewalls.

1 22. The method of claim 21, wherein,
2 the plurality of sidewalls provide a diffusion barrier
3 and an etch stop.

1 23. The method of claim 22, wherein,
2 the plurality of sidewalls protect the first material
3 under the plurality of sidewalls from being etched during the
4 etching of the first material.

1 24. The method of claim 22, wherein,
2 the plurality of sidewalls protect the second material
3 under the plurality of sidewalls from being etched during the
4 etching of the second material.

1 25. The method of claim 22, wherein,
2 the plurality of sidewalls protect the first material
3 and the second material under the plurality of sidewalls from
4 being etched during the vertical etching of the first
5 material and the second material.

1 26. The method of claim 22, wherein,
2 the plurality of sidewalls protect the first material or
3 the second material under the plurality of sidewalls from
4 being etched during the vertical etching of the first
5 material or the second material.

1 27. A method of processing for a semiconductor device,
2 the method comprising:
3 providing a substrate of the semiconductor device;

4 forming a plurality of sidewalls above a surface of the
5 substrate;
6 vertically etching horizontal surfaces of a material
7 located around the plurality of sidewalls; and
8 diffusing a dopant around the plurality of sidewalls.

1 28. The method of claim 27, wherein,
2 the plurality of sidewalls are formed by
3 forming a plurality of cylindrical pedestals above
4 a surface of the substrate,
5 depositing a sidewall material layer over the
6 cylindrical pedestals and the substrate,
7 vertically etching the horizontal surfaces of the
8 sidewall material, and
9 etching away the plurality of cylindrical
10 pedestals.

1 29. The method of claim 27, wherein,
2 the vertical etching of horizontal surfaces of the
3 material located around the plurality of sidewalls is
4 performed using a substantially anisotropic etchant.

1 30. The method of claim 27, wherein,
2 the plurality of sidewalls provide an etch stop and a
3 diffusion barrier.

1 31. The method of claim 30, wherein,

the plurality of sidewalls protect the material under the plurality of sidewalls from being etched during the etching of the material around the plurality of sidewalls and the plurality of sidewalls protect the material under the plurality of sidewalls from receiving the dopant during the diffusing of the dopant around the plurality of sidewalls.

32. A method of processing for a semiconductor device, the method comprising:

providing a substrate of the semiconductor device;
forming a plurality of sidewalls above a surface of the substrate; and
diffusing a dopant around the plurality of sidewalls.

33. The method of claim 32, wherein,
the plurality of sidewalls provide a diffusion barrier.

34. The method of claim 32, wherein,
the plurality of sidewalls are formed by
forming a plurality of cylindrical pedestals above a surface of the substrate,
depositing a sidewall material layer over the cylindrical pedestals and the substrate,
vertically etching the horizontal surfaces of the sidewall material, and
etching away the plurality of cylindrical pedestals.

1 35. The method of claim 32, further comprising:
2 vertically etching horizontal surfaces of a material
3 located around the plurality of sidewalls.

1 36. The method of claim 35, wherein,
2 the plurality of sidewalls provide an etch stop and a
3 diffusion barrier.

1 37. The method of claim 35, wherein,
2 the vertical etching of horizontal surfaces of the
3 material located around the plurality of sidewalls is
4 performed using a substantially anisotropic etchant.

1 38. The method of claim 36, wherein,
2 the plurality of sidewalls protect the material under
3 the plurality of sidewalls from being etched during the
4 vertical etching of horizontal surfaces of the material
5 around the plurality of sidewalls and the plurality of
6 sidewalls protect the material under the plurality of
7 sidewalls from receiving the dopant during the diffusing of
8 the dopant around the plurality of sidewalls.

1 39. The method of claim 35, wherein,
2 the material located around the plurality of sidewalls
3 which is vertically etched is the substrate.

1 40. The method of claim 35, wherein,
2 the material located around the plurality of sidewalls
3 which is vertically etched is a layer exposed over a surface
4 of the substrate and protected under the plurality of
5 sidewalls.

1 41. A method of processing for a semiconductor device,
2 the method comprising:
3 providing a substrate of the semiconductor device;
4 forming a plurality of sidewalls above a surface of the
5 substrate; and
6 vertically etching horizontal surfaces of a material
7 located around the plurality of sidewalls.

1 42. The method of claim 41, wherein,
2 the plurality of sidewalls provide an etch stop.

1 43. The method of claim 41, wherein,
2 the material located around the plurality of sidewalls
3 which is horizontally etched is the substrate.

1 44. The method of claim 41, wherein,
2 the material located around the plurality of sidewalls
3 which is horizontally etched is an epitaxial layer of the
4 substrate.

1 45. The method of claim 41, wherein,
2 the material located around the plurality of sidewalls
3 which is horizontally etched is a layer exposed over a
4 surface of the substrate and protected under the plurality of
5 sidewalls.

1 46. The method of claim 41, wherein,
2 the vertical etching of horizontal surfaces of the
3 material located around the plurality of sidewalls is
4 performed using a substantially anisotropic etchant.

1 47. The method of claim 41, wherein,
2 the plurality of sidewalls are formed by
3 forming a plurality of cylindrical pedestals above
4 a surface of the substrate,
5 depositing a sidewall material layer over the
6 cylindrical pedestals and the substrate,
7 vertically etching the horizontal surfaces of the
8 sidewall material, and
9 etching away the plurality of cylindrical
10 pedestals.

1 48. The method of claim 41, further comprising:
2 diffusing a dopant around the plurality of sidewalls.

1 49. The method of claim 48, wherein,

2 the plurality of sidewalls provide an etch stop and a
3 diffusion barrier.

1 50. The method of claim 49, wherein,
2 the plurality of sidewalls protect the material under
3 the plurality of sidewalls from being etched during the
4 vertical etching of the material located around the plurality
5 of sidewalls and the plurality of sidewalls protect the
6 material under the plurality of sidewalls from receiving the
7 dopant during the diffusing of the dopant around the
8 plurality of sidewalls.

1 51. The method of claim 48, wherein,
2 the dopant is diffused into the substrate around the
3 plurality of sidewalls.

1 52. The method of claim 48, wherein,
2 the dopant is diffused into the material around the
3 plurality of sidewalls.

1 53. A semiconductor device, comprising:
2 a substrate;
3 a plurality of sidewalls above a surface of the
4 substrate;
5 a dopant implanted around the plurality of sidewalls;
6 and

7 wherein the plurality of sidewalls provide a diffusion
8 barrier and protect the dopant from being implanted
9 underneath the plurality of sidewalls.

1 54. The semiconductor device of claim 53, further
2 comprising:

3 a trench etched into the substrate and through a
4 material located on the substrate around the plurality of
5 sidewalls; and

6 wherein the plurality of sidewalls provide an etch stop
7 and protect the substrate and the material underneath the
8 plurality of sidewalls from being etched.

1 55. The semiconductor device of claim 53, further
2 comprising:

3 a trench etched into the substrate around the plurality
4 of sidewalls; and

5 wherein the plurality of sidewalls provide an etch stop
6 and protect the substrate underneath the plurality of
7 sidewalls from being etched.

1 56. A semiconductor device, comprising:

2 a substrate;

3 a plurality of sidewalls above a surface of the
4 substrate;

5 a trench etched around the plurality of sidewalls; and

6 wherein the plurality of sidewalls provide an etch stop
7 and protect the substrate underneath the plurality of
8 sidewalls from being etched.

1 57. The semiconductor device of claim 56, further
2 comprising:

3 a dopant implanted around the plurality of sidewalls;
4 and

5 wherein the plurality of sidewalls provide a diffusion
6 barrier and protect the dopant from being implanted
7 underneath the plurality of sidewalls.

1 58. A system for manufacturing a semiconductor device
2 comprising:

3 a container for receiving a semiconductor wafer;
4 the semiconductor wafer having a plurality of sidewalls
5 formed over a substrate;

6 a means for etching a material around the plurality of
7 sidewalls; and

8 wherein the plurality of sidewalls provide an etch stop
9 to protect the material underneath the plurality of sidewalls
10 from being etched.

1 59. The system of claim 58, wherein,

2 the means for etching the material is a gas, plasma, or
3 liquid.

1 60. The system of claim 58, wherein,
2 the means for etching includes an excitation field to
3 excite ions in a gas, plasma, or liquid.

1 61. The system of claim 58, further comprising:
2 a means for diffusing dopants into a material around the
3 plurality of sidewalls; and
4 wherein the plurality of sidewalls provide a diffusion
5 barrier to protect the material underneath the plurality of
6 sidewalls from being implanted.

1 62. The system of claim 61, wherein,
2 the means for diffusing dopants in the material is a
3 gas, plasma, or liquid.

1 63. The system of claim 58, wherein,
2 the container is a chamber, an oven, or a bath tub.

1 64. A system for manufacturing a semiconductor device
2 comprising:
3 a container for receiving a semiconductor wafer;
4 the semiconductor wafer having a plurality of sidewalls
5 formed over a substrate;
6 a means for diffusing a dopant into a material around
7 the plurality of sidewalls; and

8 wherein the plurality of sidewalls provide a diffusion
9 barrier to protect the material underneath the plurality of
10 sidewalls from being implanted.

1 65. The system of claim 64, wherein,
2 the means for diffusing dopants into the material is a
3 gas, plasma, or liquid.

1 66. The system of claim 64, wherein,
2 the means for diffusing includes an excitation field to
3 implant the dopant into the material around the plurality of
4 sidewalls.

1 67. The system of claim 64, wherein,
2 the means for diffusing includes a source of heat to
3 diffuse the dopant into the material around the plurality of
4 sidewalls.

1 68. The system of claim 64, wherein,
2 the source of heat is an oven.

1 69. The system of claim 64, further comprising:
2 a means for etching into a material around the plurality
3 of sidewalls; and
4 wherein the plurality of sidewalls provide an etch stop
5 to protect the material underneath the plurality of sidewalls
6 from being etched.

[illegible][illegible]

	1980	1981	1982	1983	1984	1985	1986	1987	1988	1989	1990	1991	1992	1993	1994	1995	1996	1997	1998	1999	2000	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030	2031	2032	2033	2034	2035	2036	2037	2038	2039	2040	2041	2042	2043	2044	2045	2046	2047	2048	2049	2050	2051	2052	2053	2054	2055	2056	2057	2058	2059	2060	2061	2062	2063	2064	2065	2066	2067	2068	2069	2070	2071	2072	2073	2074	2075	2076	2077	2078	2079	2080	2081	2082	2083	2084	2085	2086	2087	2088	2089	2090	2091	2092	2093	2094	2095	2096	2097	2098	2099	2100	2101	2102	2103	2104	2105	2106	2107	2108	2109	2110	2111	2112	2113	2114	2115	2116	2117	2118	2119	2120	2121	2122	2123	2124	2125	2126	2127	2128	2129	2130	2131	2132	2133	2134	2135	2136	2137	2138	2139	2140	2141	2142	2143	2144	2145	2146	2147	2148	2149	2150	2151	2152	2153	2154	2155	2156	2157	2158	2159	2160	2161	2162	2163	2164	2165	2166	2167	2168	2169	2170	2171	2172	2173	2174	2175	2176	2177	2178	2179	2180	2181	2182	2183	2184	2185	2186	2187	2188	2189	2190	2191	2192	2193	2194	2195	2196	2197	2198	2199	2200	2201	2202	2203	2204	2205	2206	2207	2208	2209	2210	2211	2212	2213	2214	2215	2216	2217	2218	2219	2220	2221	2222	2223	2224	2225	2226	2227	2228	2229	2230	2231	2232	2233	2234	2235	2236	2237	2238	2239	2240	2241	2242	2243	2244	2245	2246	2247	2248	2249	2250	2251	2252	2253	2254	2255	2256	2257	2258	2259	2260	2261	2262	2263	2264	2265	2266	2267	2268	2269	2270	2271	2272	2273	2274	2275	2276	2277	2278	2279	2280	2281	2282	2283	2284	2285	2286	2287	2288	2289	2290	2291	2292	2293	2294	2295	2296	2297	2298	2299	2300	2301	2302	2303	2304	2305	2306	2307	2308	2309	2310	2311	2312	2313	2314	2315	2316	2317	2318	2319	2320	2321	2322	2323	2324	2325	2326	2327	2328	2329	2330	2331	2332	2333	2334	2335	2336	2337	2338	2339	2340	2341	2342	2343	2344	2345	2346	2347	2348	2349	2350	2351	2352	2353	2354	2355	2356	2357	2358	2359	2360	2361	2362	2363	2364	2365	2366	2367	2368	2369	2370	2371	2372	2373	2374	2375	2376	2377	2378	2379	2380	2381	2382	2383	2384	2385	2386	2387	2388	2389	2390	2391	2392	2393	2394	2395	2396	2397	2398	2399	2400	2401	2402	2403	2404	2405	2406	2407	2408	2409	2410	2411	2412	2413	2414	2415	2416	2417	2418	2419	2420	2421	2422	2423	2424	2425	2426	2427	2428	2429	2430	2431	2432	2
--	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	---